IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Guy L. STEELE, Jr.	)	Group Art Unit: 2193
	)	
Application No.: 10/035,595	)	Examiner: Mai, Tan V
	)	
Filed: December 28, 2001	)	
	)	
For: FLOATING POINT ADDER WITH EMBEDDED STATUS INFORMATION	)	Confirmation No.: 2867

Attention: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

REPLY BRIEF

Pursuant to the provisions of 37 C.F.R. § 41.41 and M.P.E.P. § 1207.03(V), Appellant requests that this appeal be maintained, for the reasons set forth in this Reply Brief, filed in response to the Examiner's Answer mailed December 27, 2006. This Reply Brief is being timely filed within two months of the Examiner's Answer.

If any fees are required, Appellant requests that the required fees be charged to Deposit Account No. 06-0916.

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I. STATUS OF CLAIMS

Claims 1-40 remain pending and under current examination. Claims 1-5 and 7-40 are subject to this Appeal.[1]

[1] Claim 6 is objected to as allowable if rewritten in independent form.

II. GROUNDS OF REJECTION TO BE REVIEWED

A. Claims 1-5 and 7-40 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,995,991 to Huang et al. ("Huang").

B. Claims 1-5 and 7-40 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,009,511 to Lynch et al. ("Lynch").

III. ARGUMENT

This Reply Brief supplements the Appeal Brief filed April 7, 2006 by responding to the Examiner's Answer mailed December 27, 2006 that included new grounds of rejection. This Reply Brief responds to the Examiner's new arguments, where appropriate, and to the new rejections in the Examiner's Answer.

A. The new rejection of claims 1-5 and 7-40 under 35 U.S.C. § 102(b) as being anticipated by Huang

The rejection of claims 1-5 and 7-40 under § 102 as anticipated by Huang is incorrect for the same reasons set forth in Appellant's appeal brief in response to the previous rejection of claims 1-5 and 7-40 under § 103 based on Huang, in which Appellants specifically pointed out the elements of claims 1-5 and 7-40 which are not taught by Huang.

With respect to claim 1, as best understood by Appellant, the Examiner alleges that Huang's X register 116 (Fig. 4) constitutes the claimed "operand" and that Huang's X_tag 116-2 constitutes the claimed "status." Examiner's Answer at 14. These allegations are incorrect. Stated simply, a register is not an "operand," as recited by claim 1. A register is hardware—a device that stores information. In contrast, an operand is a quantity on which a mathematical operation is performed. Therefore, Huang's register 116 does not constitute the claimed "operand."

Moreover, Huang's operand portion 116-1 does not constitute the claimed "operand." As clearly illustrated in Fig. 4 of Huang, the x_tag 116-2 (alleged status) is separate from operand portion 116-1, not "embedded" within the operand, as recited by claim 1.

Furthermore, the Examiner's allegations regarding claims 1-5 and 7-40 are not clear. The Examiner states "Although the tag generator (150) [of Huang] to generate the tag value separately from the output of arithmetic section (114), the examiner believes that the resulting status 'tag value' embedded within the 'resulting floating point operand'. It is noted that the format [resulting status embedded within the resulting floating point operand data] of **stored data** in the MEMORY (REGISTER FILE) 112 is the **same as** the format [status data within the floating point operand] of **data transferred** to 'X' or 'Y' register because the **read out / write in data** is usually unchanged. Therefore, the **stored** 'resulting floating point operand' includes the 'resulting status' as claimed." Examiner's Answer at 14 (emphasis in original). These new allegations cannot be understood. Claim 1 contains no recitation of a "format." Moreover, the Examiner concedes that the tag value is generated separately from the operand. Id. The Examiner's "belief" does not cure this concession, nor does it constitute a teaching or suggestion by Huang of each and every element recited by claim 1.

Because the Examiner generally references Huang's tag generator 150, Appellant points out that, contrary to the claimed structure, tag generator 150 of Huang generates the tag (alleged status) separately from the operand generator 122, and that the tag value is stored separately in x_tag 116-2 from operand portion 116-1. As noted above, the Examiner concedes this. Examiner's Answer at 14. Therefore, Huang's Fig. 4 illustrates that the "resulting status" is not "embedded within the resulting floating point operand," as recited by claim 1 (emphasis added), either at generation or during storage.

In the Examiner's Answer, the Examiner rejects claim 2 by asserting: "The memory (register file) 112 in Huang's Fig. 4 corresponds to the claimed 'operand buffer' . . . ." Examiner's Answer at 5. Even assuming Huang's register file 112 could constitute an operand buffer, Huang fails to teach or suggest a "second operand buffer", nor has the Examiner pointed to any such teachings of Huang. Moreover, the Examiner alleges "Huang et al's **arithmetic calculation circuit (100)** , specifically arithmetic section 114 inherently includes circuit(s) for determining the first / second status as claimed." Examiner's Answer at 5 (emphasis in original). The Examiner thus appears to assert that the claimed "first operand analysis circuit" and "second operand analysis circuit" of claim 2 are inherent in Huang.

Regarding inherency, M.P.E.P. § 2112 instructs: "The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic" (emphasis in original). Rather, "the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Id. (emphasis in original). The Examiner has not provided any basis in fact or technical reasoning to support his general allegation that the claimed elements are inherent in the disclosure Huang. Accordingly, the Examiner's reliance on inherency is improper and the rejection of claim 2 should be withdrawn.

The basis for the Examiner's rejection of claim 3 is not clear. Claim 3 recites determining "the first status and the second status . . . without regard to memory storage external to the first operand buffer and the second operand buffer." In the Examiner's Answer, the Examiner alleges: "Huang et al disclose a similar feature, i.e.,

'X and Y operand registers each includes a special operand indicator which is stored a special operand of a predetermine set of special operands feature". Examiner's Answer at 5. As best understood by Appellant, the Examiner alleges that Huang's X register 116 and Y register 118 correspond to the claimed "operand buffers" (Id.). However, in rejecting claim 2, the Examiner had alleged Huang's register file 112 constitutes the claimed "operand buffers". Id. Either way, Huang's register file 112 (alleged operand buffer) is "memory storage external" to x_tag 116-2, which Huang allegedly uses to determine a status, and therefore cannot constitute the claimed determining "the first status and the second status . . . without regard to memory storage external to the first operand buffer and the second operand buffer," as recited by claim 3 (emphasis added).

The basis for the Examiner's rejection of claim 4 is also not clear. Claim 4 recites determining "[the first and the second status . . . without regard to] a floating point status register." The Examiner asserts: "Huang et al. disclose special floating point operands, thus the register file 112 includes floating point registers (for storing status information e.g. of output of 150)." Examiner's Answer at 5. Huang does not teach or suggest that register 112 contains floating point registers, as asserted by the Examiner. Moreover, even assuming Huang did teach use of floating point registers within register file 112, such a teaching would be the opposite of determining "[the first and the second status . . . without regard to] a floating point status register," as recited by claim 4 (emphasis added).

The Examiner summarily rejects claim 5, alleging "Huang et al's arithmetic section 114[], tag generator 150 and special operand generator 122 in combination provide the 'resulting floating point operand and embed the resulting status' as claimed,

since they produce the resulting floating point operand along with the resulting tag to be stored within the register file 112 . . . ." Examiner's Answer at 6. It is not clear how this allegation relates to claim 5. The Examiner has not identified any teachings of Huang that allegedly disclose the claimed "adder circuit," "adder logic circuit," and "result assembler," as recited by claim 5. Moreover, as discussed above, Huang does not teach or suggest embedding "the resulting status within the resulting floating point operand," as recited by claim 5.

Claims 7-14 are allowable at least because claims 7-14 depend from allowable claim 1. The Examiner summarily rejects claims 9-14 by providing a number of citations to Huang. However, none of these portions of Huang teach or suggest:

(1) an "overflow status [that] represents one in a group of a +OV status and a –OV status," as recited by claim 9;

(2) an "overflow status . . . represented as a predetermined non-infinity numerical value," as recited by claim 10;

(3) an "underflow status [that] represents one in a group of a +UV status and a – UV status," as recited by claim 11; or

(4) an "underflow status [] represented as a predetermined non-zero numerical value," as recited by claim 12.

Independent claims 15 and 28, although of different scope than claim 1, patentably distinguish from Huang for at least the same reasons as claim 1. Claims 16-27 and 29-40 depend from independent claims 15 and 28 and therefore include all of the elements recited therein. Dependent claims 16-27 and 29-40 are also allowable for the same reasons discussed above with respect to claims 2-5 and 7-14. Accordingly, Huang cannot anticipate claims 1-5 and 7-40. Appellant requests the Board to overturn the rejection of claims 1-5 and 7-40.

B. The rejection of claims 1-5 and 7-40 under 35 U.S.C. § 103(a) as being unpatentable over Lynch

In the Examiner's Answer, discussing Lynch, the Examiner states: "the examiner interprets the floating point register within the register stack as an operand." Examiner's Answer at 15. As discussed above, (1) neither a hardware register stack nor a register can constitute the claimed "operand;" (2) Lynch does not teach or suggest the claimed "resulting status embedded within the resulting floating point operand," and (3) Lynch suffers from the same drawbacks of the prior art discussed in Appellant's specification. Independent claims 15 and 28, although of different scope than claim 1, patentably distinguish from Lynch for at least the same reasons as claim 1.

In the Examiner's Answer, as with the rejection based on Huang discussed above, the Examiner has failed to address each and every element recited by claims 2-5 and 7-40. The Examiner's rejects claims 2-5 and 7 by making general assertions that Lynch "should" include these elements and that these elements are "inherent". Examiner's Answer at 8-9. As discussed above, the Examiner has not provided any basis in fact or technical reasoning to support his general allegation that the claimed elements are inherent in the disclosure Lynch. Moreover, the Examiner's general assertion that Lynch "should have" the claimed elements does not support a rejection under § 103(a). Accordingly, the Examiner's rejection of claims 2-5 and 7 should be withdrawn. Dependent claims 16-20 and 29-33 are allowable for at least the same reasons as claims 2-5 and 7.

Regarding claims 9-14, 22-27, and 35-40, the Examiner merely alleges: "Lynch teaches the claimed 'status' information, e.g., '[t]ypes of special floating point numbers

include zero, +infinity, -infinity, and NaNs' (col. 17, lines 6-7) and Fig. 5. In col. 18, first complete paragraph, Lynch discloses '+infinity' & '-infinity' features as Appellant's claim 14." Examiner's Answer at 15. The Examiner has not shown that Lynch teaches at least:

(1) the claimed "overflow status . . . represented as a predetermined non-infinity numerical value," as recited by claim 10;

(2) the claimed "underflow status [that] represents one in a group of a +UV status and a – UV status," as recited by claim 11; or

(3) the claimed "underflow status [] represented as a predetermined non-zero numerical value," as recited by claim 12.

Accordingly, no *prima facie* case of obviousness has been established for claims 1-5 and 7-40.

IV. CONCLUSION

The additional reasons given above supplement, in response to the Examiner's Answer, those presented in the Appeal Brief filed on April 7, 2006 and demonstrate that pending claims 1-40 are allowable. Appellant respectfully requests that the Board reverse the Examiner's rejections.

If any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Reply Brief, Appellant requests such an extension. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 that are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 20, 2007

By: _____
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